

Amendment and Response

Applicant: Jong-Hoon Oh

Serial No.: 10/820,292

Filed: April 8, 2004

Docket No.: I436.106.101/IO040408PUS (Previously I331.141.101)

Title: MULTICHIP PACKAGE WITH CLOCK FREQUENCY ADJUSTMENT

IN THE CLAIMS

Please amend claims 6, 12, and 20 as follows:

1. (Original) A multi-chip package comprising:
a memory device receiving a clock signal having a frequency, the memory device operating at the clock signal frequency and including a temperature sensor providing a temperature signal representative of a temperature of the memory device; and
a logic device providing the clock signal and receiving the temperature signal, wherein the logic device adjusts the clock signal frequency based on the temperature signal.
2. (Original) The multi-chip package of claim 1, wherein the memory device comprises a random access memory device.
3. (Original) The multi-chip package of claim 1, wherein the memory device comprises a magnetic random access memory device.
4. (Original) The multi-chip package of claim 1, wherein the logic device comprises a microprocessor.
5. (Original) The multi-chip package of claim 1, wherein the temperature signal is indicative of a junction temperature of the memory device.
6. (Currently Amended) ~~The multi-chip package of claim 1~~ A multi-chip package comprising:
a memory device receiving a clock signal having a frequency, the memory device operating at the clock signal frequency and including a temperature sensor providing a temperature signal representative of a temperature of the memory device; and

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a logic device providing the clock signal and receiving the temperature signal, wherein the logic device adjusts the clock signal frequency based on the temperature signal, and wherein the logic device provides the clock signal at a first frequency when the temperature signal indicates that the temperature of the memory device is less than a threshold temperature, and provides the clock signal at a second frequency when temperature signal indicates that the temperature of the memory device is at least equal to the threshold temperature.

7. (Original) The multi-chip package of claim 6, wherein the memory device has a rated operating frequency at a rated operating temperature, wherein the threshold temperature is substantially equal to rated operating temperature, wherein the first frequency is substantially equal to the rated operating frequency, and wherein the second frequency is less than the first frequency and at a frequency at which the memory device operates reliably at a temperature above the rated operating temperature.
8. (Original) The multi-chip package of claim 7, wherein the logic device further includes a clock generator configured to generate the clock signal.
9. (Original) The multi-chip package of claim 8, wherein the temperature sensor provides the temperature signal having a first state when the temperature of the memory device is less than rated operating temperature and having a second state when the temperature of the memory device is at least equal to the threshold temperature, and wherein the wherein the clock generator provides the clock signal at the rated operating frequency when the temperature signal has the first state and at the second frequency when the temperature signal has the second state.
10. (Original) The multi-chip package of claim 8, wherein the logic device further includes a memory controller configured to control access operations of the memory device by the logic device, wherein the temperature sensor provides the temperature signal in response to a read signal, wherein the memory controller provides the read signal and provides a flag signal having a first state when the temperature signal indicates that the memory device temperature is less

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than the rated operating temperature and a second state when the temperature signal indicates that the memory device temperature is at least equal to the rated operating temperature, and wherein the wherein the clock generator provides the clock signal at the rated operating frequency when the flag signal has the first state and at the second frequency when the flag signal has the second state, and wherein the memory controller provides a wait signal representative of whether an access operation is on-going, and wherein a timing of an adjustment of the clock signal frequency by the clock generator is based on the wait signal.

11. (Original) A clock system in a multichip package including a memory device, the clock system comprising:

a clock generator providing a clock signal having a frequency to the memory device; and
a temperature sensor providing a temperature signal representative of a temperature of the memory device, wherein the clock generator adjusts the frequency of the clock signal based on the temperature signal.

12. (Currently Amended) ~~The clock system of claim 11~~ A clock system in a multichip package including a memory device, the clock system comprising:

a clock generator providing a clock signal having a frequency to the memory device; and
a temperature sensor providing a temperature signal representative of a temperature of the memory device, wherein the clock generator adjusts the frequency of the clock signal based on the temperature signal, and wherein the clock generator provides the clock signal at a first frequency when the temperature signal indicates that the temperature of the memory device is less than a threshold temperature and at a second frequency when the temperature signal indicates that the temperature of the memory device is at least equal to the threshold temperature.

13. (Original) The clock system of claim 12, wherein the memory device has a rated operating frequency at a rated operating temperature.

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14. (Original) The clock system of claim 13, wherein the threshold temperature is substantially equal to the rated operating temperature, wherein the first frequency is substantially equal to the rated operating frequency, and wherein the second frequency is less than the first frequency and at a frequency at which the memory device operates reliably at a temperature above the rated operating temperature.

15. (Original) The clock system of claim 11, wherein multichip package includes a logic device.

16. (Original) The clock system of claim 15, wherein the logic device comprises a microprocessor.

17. (Original) The clock system of claim 11, wherein the memory device comprises a random access memory device.

18. (Original) The clock system of claim 11, wherein the memory device comprises a magnetic random access memory device.

19. (Original) A method of operating a multichip package including a memory device, the method comprising:

monitoring a temperature of the memory device; and

providing a clock signal at a first frequency to the memory device when the temperature of the memory chip is less than a threshold temperature.

20. (Currently Amended) ~~The method of claim 19, further comprising:~~ A method of operating a multichip package including a memory device, the method comprising:

monitoring a temperature of the memory device;

providing a clock signal at a first frequency to the memory device when the temperature of the memory chip is less than a threshold temperature; and

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providing the clock signal at a second frequency to the memory device when the temperature of the memory chip is at least equal to the threshold temperature, wherein the second frequency is less than the first frequency.

21. (Original) The method of claim 19, wherein monitoring a temperature of the memory device comprises monitoring a junction temperature of the memory device.
22. (Original) The method of claim 19, where the threshold temperature comprises a rated operating temperature of the memory device.
23. (Original) A multi-chip package comprising:
a random access memory chip receiving a clock signal having a frequency, the memory device operating at the clock signal frequency and including a temperature sensor providing a temperature signal representative of a junction temperature of the memory device; and
a microprocessor chip providing the clock signal and receiving the temperature signal, wherein the microprocessor chip provides the clock signal at a first frequency when the temperature signal indicates that the junction temperature is less than a rated operating temperature of the random access memory chip, and provides the clock signal at a second frequency when temperature signal indicates that the junction temperature is at least equal to the rated operating temperature of the random access memory chip.